Abstract of the Disclosure

A skew-free dual rail bus driver is provided. The dual rail bus driver includes a first driver outputting first dual signals of the same level, and outputting second dual signals of different levels when a level of a clock changes; a decoder receiving the second dual signals and outputting a single signal; a dual signal controller being triggered due to a change in the level of the second dual signals and outputting third dual signals of different levels in response to the single signal at the same time; and a second driver inverting the levels of the third dual signals output from the dual signal controller and outputting fourth dual signals in accordance with a change in the level of the clock. Accordingly, it is possible to obtain dual rail bus driving signals in which skew does not occur. Also, changes in the phases of dual signals are detected and used as a trigger signal input to an edge trigger flip-flop which is a dual signal controller. Also, signals output from the edge trigger flip-flop are used as dual rail bus driving signal, instead of using a clock delayer.

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